# INTEGRATION
the VLSI Journal

## AUTHOR INFORMATION PACK

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### DESCRIPTION

*Integration's* aim is to cover every aspect of the **VLSI** area, with an emphasis on cross-fertilization between various fields of science, and the design, verification, test and applications of **integrated circuits** and **systems**, as well as closely related topics in process and device technologies. Individual issues will feature peer-reviewed tutorials and articles as well as reviews of recent publications. The intended coverage of the journal can be assessed by examining the following (non-exclusive) list of topics:

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• FPGAs and reconfigurable computing, Application-specific processors, Microfluidics, Cyber-physical Systems
Y. Cai, Tsinghua University, Beijing, China
• Physical Design, Power Analysis, Design for manufacturability, 3D IC Design.

**B. Carrion Schafer**, University of Texas at Dallas Department of Electrical and Computer Engineering (ECE), Richardson, Texas, United States

• High-Level Synthesis, Hardware Security, Design Space Exploration, Reconfigurable Computing, FPGA (Field Programmable Gate Arrays)

**L. Cassano**, Politecnico di Milano, Milano, Italy

• Fault diagnosis and tolerance, Reconfigurable computing, Fault testing and simulation, Hardware security, Formal verification

**R. Castro-Lopez**, University of Seville, Sevilla, Spain

• Analog/RF/Mixed-Signal design automation, Analog/Mixed-Signal Modeling, Analog/RF Physical Design and Synthesis

**H. Chen,** Shanghai Jiao Tong University - Fahua Campus, Shanghai, China

• VLSI reliability; Machine learning and neuromorphic computing; Numerical analysis and modeling for VLSIs; Integrated circuit for signal and control systems.

**H. Chen,** Wright State University, Dayton, Ohio, United States

• Digital wideband receiver, Tunable band pass filter, Active inductor, VLSI testing.

**G. Dündar**, Bogazici University Department of Electrical and Electronics Engineering, Istanbul, Turkey

• Analog Integrated Circuit Design, Design Automation for Analog Circuits

**A. Fish**, Bar-Ilan University, Ramat Gan, Israel

• Energy efficient digital ICs, Hardware security, Embedded memories, Alternative logic families

**Q.J. Gu,** University of California Davis, Davis, California, United States

• Mm-Wave/THz Integrated Circuits and System, Design Techniques for post-CMOS Devices, System-on-Chip Techniques, Ultra-Low Power IC and Systems, High Performance RF/Mixed-Signal IC and System

**T.Y. Ho,** National Tsing Hua University, Hsinchu, Taiwan

• Microfluidic (lab on chip), Cyber physical system, Hardware security, Physical design

**N. Horta,** University of Lisbon, Lisbon, Portugal

• Electronic Design Automation, Analog and Mixed-Signal Design, Circuit and System Level Synthesis, Layout Synthesis, Analog IP and Reuse

**T. Ishihara,** Nagoya University, Nagoya, Japan

• Low power digital design, Optical circuit design and computing

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Fault tolerant computing, Emerging technology, Neuromorphic computing, Approximate computing, Computer architecture

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• Hardware security, Trusted IC design, Secure supply chain, Hardware-oriented cybersecurity, IoT security.

**T. Kim,** Seoul National University Department of Electrical and Computer Engineering, Seoul, Korea, Republic of

• Logic and physical synthesis, Low power design, Clock networks

**T. Kim,** University of California Riverside, Riverside, California, United States


**C.-K. Koh,** Purdue University, West Lafayette, Indiana, United States

• Physical design and circuit modeling

**M. Lanuzza,** University of Calabria, Rende, Italy

• Ultra low-voltage circuit design, Hardware security, Arithmetic circuits, Digital/analog design in emerging technologies (spintronics, TunnelFet)

**B. Li,** Technical University of Munich, Munchen, Germany

• Timing Analysis and Optimization; Statistical Modeling and Optimization; Design and Test for Microfluidic Biochips; Asynchronous Circuits; Physical Design; Hardware Security; FPGA Design and Reconfigurable Computing; Network-on-Chips

**S.P. Mohanty,** University of North Texas, Denton, Texas, United States


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• Low power IC design, Nano-scale Memory Design (CMOS, FinFET and spintronics), Biomedical IC Design, Nano-scale IC design, Analog Mixed-Signal IC Design

**S. Nakatake,** The University of Kitakyushu, Kitakyushu, Japan

• Physical design, Combinatorial algorithm, Analog layout, Analog circuit design, A/D converter, Sensor system

**N. Nedjah,** Rio de Janeiro State University, Rio de Janeiro, Brazil

• Network-on-chip, Reconfigurable hardware, Bio-inspired architectures
H. Yu, Southern University of Science and Technology, Shenzhen, China
- Low power IoT sensor design, Analog modeling and simulation, 3D-IC and emerging technology
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- Hardware security, Fault tolerance, Networks-on-Chip
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- Low power, Power and signal integrity, 3D IC, Cross-layer design and optimization, Design for reliability
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